CCD DEVELOPMENT PROGRESS AT LAWRENCE BERKELEY NATIONAL LABORATORY

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Abstract P-channel CCD imagers, 200-300 μm thick, fully depleted, and back-illuminated are being developed for scientific applications including ground- and space-based astronomy and x-ray detection. These thick devices have extended IR response, good point-spread function (PSF) and excellent radiation tolerance. Initially, these CCDs were made in-house at LBNL using 100 mm diameter wafers. Fabrication on high-resistivity 150 mm wafers is now proceeding according to a model in which the wafers are first processed at DALSA Semiconductor up to the Al contact mask step. They are then thinned and the rest of the processing is done in small batches at LBNL. Alternative approaches are also discussed. In addition we have implemented designs that permit high-voltage biasing to further improve the PSF. With these designs, operation of 200 μm thick CCDs at 100 V or more bias with excellent PSF is practical.

Key words: fully-depleted, back-illuminated, p-channel, IR response, high voltage, PSF.

1. INTRODUCTION

We have developed fully depleted, back-illuminated CCD imagers fabricated on high-resistivity, n-type silicon for scientific applications (see Holland *et al*., 2003 and Figure 1). Since first described by Holland *et al.* (1996), the virtues of such a CCD have been well established. The typical thickness of 200-300 μm results in good near-infrared quantum efficiency

(QE) and greatly reduces fringing (Groom *et al*., 1999). The point spread function (PSF) is well defined and is determined by the transit time of the photo-generated holes in an electric field that extends throughout the thickness of the device. Under full depletion conditions the PSF is directly proportional to the thickness of the CCD and inversely proportional to the square-root of the substrate bias used (Holland *et al*., 2003). The PSF of a relatively thick, fully depleted CCD can be superior to that observed with a conventional thinned CCD if the latter has a significant field-free region at the backside of the device (Bebek *et al*., 2003). Since the CCD is p-channel, the radiation hardness due to bulk damage from protons in the space environment is improved significantly (Bebek *et al*., 2002) when compared to conventional n-channel CCDs due to the lack of phosphorus-vacancy formation in the channels.

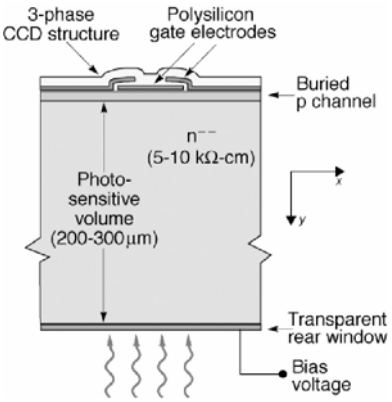

Figure 1. Schematic view of LBNL CCD showing the clock electrodes on the front surface and the bias voltage applied to the rear. These devices are operated fully depleted to achieve good PSF.

In this work we describe efforts to fabricate fully depleted, back-illuminated CCDs on 150 mm diameter wafers. Three fabrication process flows under investigation to produce high performance CCDs are discussed. In addition, we report results to date on high-voltage compatible CCDs of particular interest to the proposed SuperNova/Acceleration Probe (SNAP) satellite (http://snap.lbl.gov).

2. CCD IMAGER DEVELOPMENT AT LBNL

2.1 Historical Development

In the early days of CCD development at LBNL, fabrication was done in-house in a Class 10 clean room using 100 mm diameter wafers. Figure 2 shows such a 100 mm wafer containing a 2K x 4K, 15 μm pixel size CCD and other smaller devices. CCDs fabricated at this facility are currently in use at ground-based observatories.

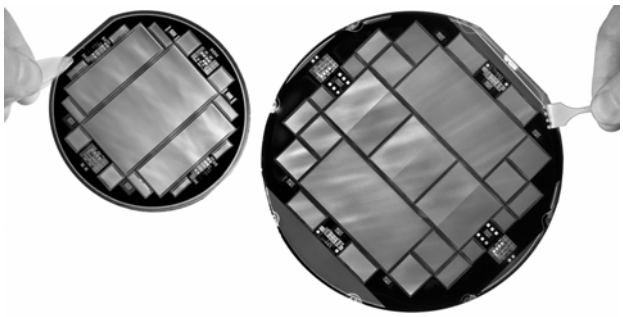

Figure 2. Photographs showing examples of CCD wafer layouts for 100 mm wafer (left) and SNAP version-0 CCD on 150 mm wafer (right).

The processing steps critical to the fabrication of LBNL CCDs and the challenges in implementing them have been described in some detail in Holland *et al.* (2003) and Bebek *et al.* (2004). In summary, they include completion at the full wafer thickness of all front-side processing up to the aluminum (Al) contact mask step. Then the wafers are ground and polished to final thickness of 200-300 μm. They are then back-side finished with an in-situ doped polycrystalline silicon (ISDP) process at 650C making an extremely thin ohmic contact for biasing. The ISDP formation process temperature is too high for Al so the contacting and metallization is done afterwards.

2.2 Expansion and Outsourcing

With the advent of the proposed SNAP it became clear that the large number of devices required for this and other applications would require the services of an outside fabrication vendor. DALSA Semiconductor was selected. Since DALSA uses 150 mm wafers, new design formats were needed. Figure 2 shows a 150 mm wafer with three SNAP style version-0

CCDs and two 2K x 4K, 15 μm CCDs. Two different pixel sizes 10.5 μm (2880^2) and 12 μm (2520^2) were chosen for the SNAP version-0 devices to accommodate early SNAP design requirements.

When the decision to outsource fabrication was made it was initially planned to execute the entire process at DALSA. It was found, at an early stage, that significant process development would be required to work with the thinned 150 mm wafers. As a result, a business model was developed in which DALSA does front-side processing up to the contacting step. LBNL then finishes the processing. To do this the LBNL clean room equipment was upgraded to 150 mm wafer capability using good quality used equipment. While a number of difficulties were encountered at first (Bebek *et al*., 2004) recent results, to be described below, are very promising. A significant advantage of the business model is that the processing necessary for back illumination is done at the wafer level, which results in a technology that is amenable to volume manufacturing.

In addition to the business model described above, two other approaches have been followed: These include the use of a refractory metal alloy (a Ti/TiN stack) instead of the standard aluminum interconnects. This material can withstand the ISDP process at 650C so the front-side can be fully completed at DALSA before thinning and back-side finishing. Although the TiN has higher resistivity than Al, good results have been obtained (Bebek *et al*., 2004).

As a second alternative process we are collaborating with researchers at the Jet Propulsion Laboratory (JPL) to apply delta doping to p-channel CCDs. Molecular beam epitaxy is used to form the backside ohmic contact layer. This is a low-temperature process that grows a thin layer of Sb-doped silicon at temperatures not exceeding 450C, thereby permitting Al interconnects to be fabricated before thinning. This process is still under development (Bebek *et al*., 2004) but continues to look promising, especially for UV-enhanced detectors.

2.3 Development of High Voltage CCDs

As the SNAP proposal evolved, further refinements in science requirements led to the specification of a pixel size of 10.5 μm together with a PSF of 4 μm rms. In addition, larger pixel counts were required. PSF measurements on the version-0 devices showed that this requirement could not be met without going to higher substrate voltages than version-0 was designed to accommodate. The version-0 devices were normally 250 μm thick and could safely withstand about 50 V of bias while PSF measurements and modeling predicted a need for 200 μm devices biased to 80 V. Figure 3 shows measured PSF data for 200 and 280 μm CCDs as a

function of substrate voltage (Karcher *et al*, 2004 with additional measurements by J. Fairfield).

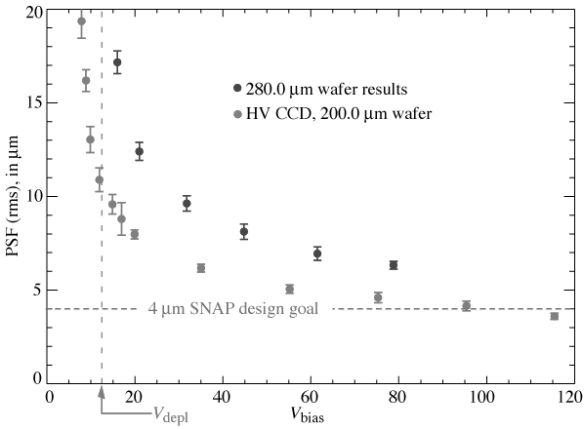

Figure 3. Graph showing measured PSF for a low-voltage CCD 280 μm thick and a high-voltage device 200 μm thick. The dashed line shows SNAP science requirement of 4 μm.

An analysis of breakdown conditions in the version-0 devices led to a number of design enhancements (S.E. Holland, private communication) resulting in the version-1 CCDs. The wafer, shown in Fig. 4a, contains four version-1 devices, all with 3512 x 3512, 10.5 μm pixels and various design modifications together with other smaller test CCDs. More than 36 of the SNAP devices were fabricated (some un-thinned, some with the business model processing and some with TiN contacting), mounted and tested to determine performance. Most of the thinned CCDs with the high-voltage enhancements withstood voltages well in excess of 80 V. Some of the un-thinned devices withstood over 200 V of bias without any noticeable breakdown or “glow”. There were some problems observed in some of the CCDs in which the signal baseline values were unstable and tended to drift under certain bias voltage and exposure conditions.

A detailed analysis of the results was made and new simulation models were introduced to explain the observed behavior. Armed with these improved models, the current SNAP version-2 CCDs were designed. These were fabricated on the wafer shown in Fig. 4b, containing four devices of the same pixel count and size as the version-1.

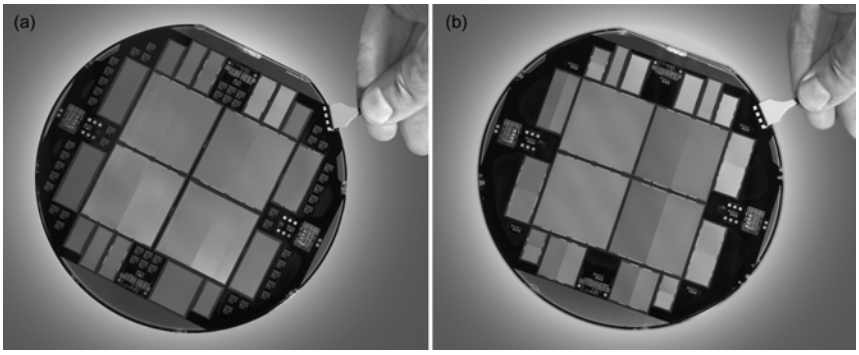

Figure 4. Wafer photographs showing (a) SNAP version-1 and (b) version-2 CCDs.

2.4 Version-2 Device Test Results

The version-2 design was submitted to DALSA in early 2005 and the first wafers were received in March. These were proof devices fully finished with Al contacting, ready to be tested un-thinned with front-illumination. All the version-2 CCDs were wafer probed at -45C and tested for functionality prior to dicing. This was done at UC Lick with the help of Richard Stover and will soon be performed at LBNL when our own wafer prober commissioning is complete. Of 16 devices, about 80% were functional, and after mounting, most of those tested were found to perform well in our test dewar operated around 140 K.

An important goal of the version-2 design is to achieve reliable operation at the SNAP-required substrate voltage V_{sub} = 80 V. In order to test this, CCD performance was evaluated at voltages significantly higher than required. For example, Fig. 5 shows an 1800 second dark exposure of one of the un-thinned CCDs operated at V_{sub} = 206 V. At this voltage the CCD is fully depleted even though it is 650 µm thick. This can be seen by examining the cosmic ray tracks. Incomplete depletion leads to puffy track ends from diffusion in field-free regions. No evidence of "glow" or any other signs of breakdown were observed, and in fact, the dark current measured for this image was determined to be 0.63 e^-/pixel/hour.

To measure gain and charge transfer efficiency (CTE), x-rays from the radioactive source ^{55}Fe are used (Janesick, 2001). Figure 6a shows the x-ray histogram obtained from such a measurement of a different front-illuminated version-2 CCD operated at V_{sub} = 107 V. The well resolved K_α and K_β x-ray peaks are an indicator of good performance. The read noise for this CCD

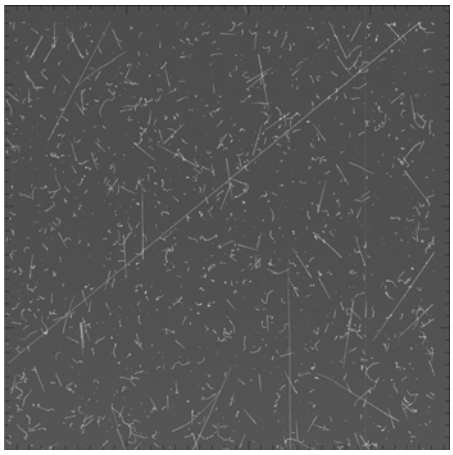

Figure 5. 1800 second dark exposure of a 650 µm thick front illuminated CCD operated fully depleted at V_{sub} = 206 V.

was 3.6 e^- rms (at 70k pixels/sec). In Fig. 6b is shown the parallel stacking plot for the same measurement. This and the corresponding serial plot yielded a serial CTE = 0.999 999 75 $\pm 1.4\times10^{-7}$ and a parallel CTE = 0.999 999 88 $\pm$ 1.2×10^{-7}.

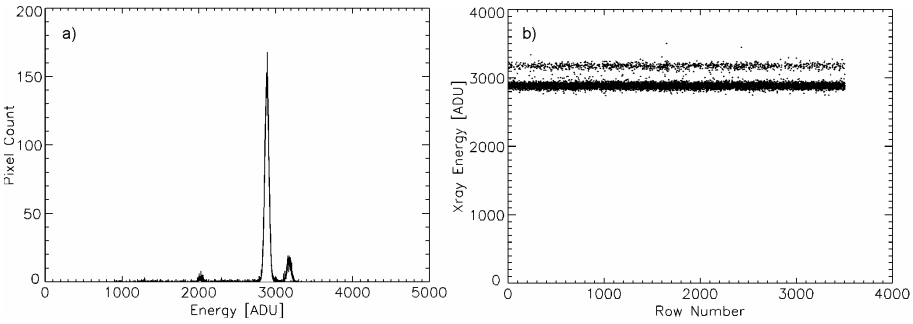

Figure 6. ^{55}Fe x-ray histogram (a) and parallel stacking plot (b) for front-illuminated SNAP version-2 CCD operated at V_{sub} = 107 V.

In addition to the full wafer thickness front-illuminated CCDs, a number of thinned and finished devices have been produced according to the business model and screened with wafer cold-probing (over 40, 200 µm thick CCDs to date). At the time of writing, only a couple of the SNAP version-2 CCDs have been tested. The promising results so far are illustrated in the projected test image shown in Fig. 7.

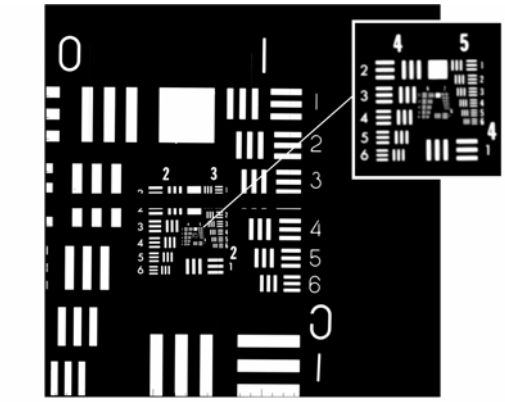

Figure 7. Image of USAF resolution test pattern projected on 200 μm thick finished CCD operated at V_{sub} = 206 V and read out via two amplifiers. Horizontal dark band along the center line is overscan. Inset shows magnified view of central portion of image.

3. ACKNOWLEDGEMENTS

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REFERENCES

Bebek, C.J. *et al.*, 2002, Proton radiation damage in p-channel CCDs fabricated on high-resistivity silicon, IEEE Trans. on Nucl. Sci., **49**: 1221-1225.

Bebek, C.J. *et al.*, 2003, Fully depleted back-illuminated p-channel CCD development, *Proc. SPIE* **5167**:50-62.

Bebek, C.J., *et al*., 2004, Development of fully depleted back-illuminated charge coupled devices, *Proc. SPIE* **5499**:140-150.

Holland, S.E., *et al*., 1996, A 200 x 200 CCD image sensor fabricated on high-resistivity silicon, in *IEDM-1996 Technical Digest*, pp. 911-914.

Holland, S.E., *et al*., 2003, Fully depleted, back-illuminated charge-coupled devices fabricated on high-resistivity silicon, *IEEE Trans. Elec. Dev.*, **50**:225-238.

Groom, D.E., *et al*., 1999, Quantum efficiency of a back-illuminated CCD imager: an optical approach, *Proc. SPIE*, **3649**:80-90.

Karcher, A. *et al*., 2004, Measurement of lateral charge diffusion in thick, fully depleted, back-illuminated CCDs, IEEE Trans. on Nucl. Sci., **51**: 2231.

Janesick, J., 2001 Scientific Charge Coupled Devices, SPIE, Bellingham, WA.